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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/659,885	09/12/2000	Paolo Menegoli	850063.498D2	2853

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EXAMINER
LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/659,885	Applicant(s) MENEGOLI, PAOLO	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Claims 21, 22, 23, 24 and 25 are objected to because of the following informalities: Since there are two source regions in claim 21, it is unclear whether the word "region" (line 16 of claim 21) is being referred to "regions". Claim 22, line 5, it is unclear whether the deep barrier region located between the epitaxial layer and the substrate. Claim 23, line 9, "IC" should be in full form instead of in abbreviation. Claims 24, 25, line 3, "a first conductivity type" is unclear whether it is being referred to "the first conductivity type". Appropriate correction is required.

2. Claims 17-25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification discloses a lateral DMOS transistor in fig. 18. The specification never discloses a vertical DMOS transistor as claimed in claims 17 and 21-25.

The specification never discloses diverting current from the body-to-drain pn junction of the DMOS transistor with the Schottky diode that is co-integrated with the DMOS transistor when the source becomes more positive than a drain of the DMOS transistor and the gate has not induced a channel region between the source region and the drain region as claimed in claim 17.

The specification never discloses a plurality of insulated gate electrodes formed over the outer portions and inner central portions of the first and second source regions, respectively, as claimed in claim 22.

3. Claims 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Since claim 17 discloses the current being divert from the body-to-drain pn junction of the DMOS transistor, it is unclear how the current also diverts from a source of the DMOS transistor in claims 18, 19 and 20.

In claim 19, lines 2-3, the phrase "a p-n junction body diode" is unclear whether it is similar to the "pn junction diode" of claim 17.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 17-20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cogan in view of Pearce.

In regards to claim 17, Cogan discloses a DMOS transistor in figs. 6 and 7 and in column 4, lines 25-56 of the written description. It comprises: a method of operating a DMOS transistor [90] in an integrated circuit, the transistor having a drain [100, 102] of first conductivity, a body [91] formed of second conductivity in an epitaxial layer [102] of first conductivity to form a pn junction diode with the drain, a source [92] of first conductivity in the body, a gate electrode [96] positioned above the source, the body, and the epitaxial layer, a conductive contact (drain terminal) coupled to the drain, and a metallic source contact [110] coupled to the source and to the epitaxial layer to form a

Schottky diode, comprising diverting current from the body-to-drain pn junction of the DMOS transistor with a Schottky diode [110, 102] that is co-integrated with the DMOS transistor when the source [92] becomes more positive than a drain [102] of the DMOS transistor and the gate has not induced a channel region between the source region and the drain region (the transistor [90] is shut off when a load which transistor [90] is switching is inductive).

Cogan differs from the claimed invention by not showing the drain of first conductivity formed in a buried region of same conductivity.

Pearce shows a drain [34] of first conductivity formed in a buried region [32] of same conductivity in fig. 2.

Since both Cogan and Pearce teach an insulated gate transistor with a drain, it would have been obvious to have the buried region of Pearce in Cogan because it depends on the design of the circuit and it improves the flow of the drain current to the top surface of the device.

In regards to claim 18, Cogan differs from the claimed invention by not showing the act of diverting current from the body-to-drain pn junction of the DMOS transistor includes diverting current from a parasitic bipolar transistor having a collector coupled to a substrate in which both the DMOS transistor and the Schottky diode are integrated.

Pearce shows an n-channel type lateral DMOS transistor formed on a p-type substrate in fig. 2.

Since both Cogan and Pearce teach an n-channel type DMOS transistor with a lateral channel region, it would have been obvious to have the p-type supporting substrate of Pearce in Cogan because it provides support for a transistor.

The combined device of Cogan and Pearce would inherently show the act of diverting current from the body-to-drain junction of the DMOS transistor includes diverting current from a parasitic bipolar transistor having a collector coupled to a substrate in which both the DMOS transistor and the Schottky diode are integrated.

In regards to claim 19, the combined device of Cogan and Pearce shows the act of diverting current from the body-to-drain pn junction of the DMOS transistor with a Schottky diode includes diverting current from a p-n junction body diode [91, 102] having a cathode coupled to the drain [102] and an anode coupled to the source [92].

In regards to claim 20, the combined device of Cogan and Pearce shows the act of diverting current from the body-to-drain pn junction of the DMOS transistor with a Schottky diode includes diverting current from the body-to-drain pn junction with a Schottky diode having a cathode coupled to the drain [102] and an anode coupled to the source [92].

In regards to claim 24, Cogan discloses a DMOS transistor and a method of operating a DMOS transistor in an integrated circuit in figs. 6 and 7 and in column 4, lines 25-56 of the written description. The DMOS transistor including an epitaxial layer [102] of a first conductivity type; a drain region [102] of the first conductivity type formed within the epitaxial layer; a body region [91] of a second conductivity type formed within the epitaxial layer and forming a pn junction diode [91, 102] with the drain region; a

source region [92] of the first conductivity type formed within the body region; a gate electrode [96] positioned above the source region, the body region, and the epitaxial layer; a conductive drain contact (a drain terminal) coupled to the drain region; and a metallic source contact [110] coupled to the source region and to the epitaxial layer, the metallic source contact having contact with the epitaxial layer at a surface of contact, the surface of contact forming a rectifying barrier in the form of a Schottky diode, the method of operating comprising: conducting current through the Schottky diode when a forward bias is applied from the metallic source contact to the conductive drain contact.

Cogan differs from the claimed invention by not showing an epitaxial layer of a first conductivity type formed over a substrate of a second conductivity type.

Pearce shows an epitaxial layer [34] of a first conductivity type formed over a substrate [30] of a second conductivity type in fig. 2.

Since both Cogan and Pearce teach an n-channel type DMOS transistor with a lateral channel region, it would have been obvious to have the p-type supporting substrate of Pearce in Cogan because it provides support for a transistor.

6. Applicant's arguments filed 9/27/02 have been fully considered but they are not persuasive.

It is urged, in page 5 of the remarks, that Cogan does not account for the effects of parasitic BJT's associated with a power DMOS structure on an integrated circuit having many other transistors on same substrate. However, the combined device of Cogan and Pearce inherently show the act of diverting current from the body-to-drain junction of the DMOS transistor includes diverting current from a parasitic bipolar transistor

having a collector coupled to a substrate in which both the DMOS transistor and the Schottky diode are integrated. Since current is being divert by the Schottky diode, the effects of parasitic BJT's associated with a power DMOS structure on an integrated circuit having many other transistors on same substrate would be reduced.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
October 21, 2002

Steven Loke